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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,716	09/30/2003	Robert H. Utley	3	6315

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EXAMINER	
FRANKLIN, RICHARD B	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,716	UTLEY, ROBERT H.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
8/7/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 5 and 7 – 20 have been examined.

Response to Arguments

2. Applicant's arguments filed 02 June 2006 have been fully considered but they are not persuasive.

Applicant argues that the relied upon reference, US Patent No. 5,764,641 (hereinafter Lin), does not teach or suggest maintaining separate discarded data block indicators for respective ones of the plurality of input ports (See remarks; Pages 6 and 7). Applicant also alleges that the teachings of Lin teach away from the claimed limitation (See remarks; Page 7). However, Applicant has failed to state how Lin teaches away from the claimed limitation.

The Examiner submits that Lin does teach the above claimed limitation. Lin teaches "the controller sets an EPD flag that is associated with the virtual circuit identified in the cell (Items 111 – 112)" (Lin; Col 6 Lines 59 – 61). This teaching of Lin suggests maintaining EPD flags for each virtual circuit in the system because in order to set the EPD flag associated with the virtual circuit, there must be separate EPD flags associated with each virtual circuit.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 5 and 7 – 20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,764,641 (hereinafter Lin).

As per claims 1 and 19 – 20, Lin teaches a processor comprising (Figure 1 Item 10): a plurality of input ports (Figure 1 Item 12, Col 4 Lines 51 – 58); memory circuitry (Figure 1 Item 14, Col 4 Lines 51 – 58) for storing data blocks associated with protocol data units and received by the processor at the input ports; and controller circuitry (Figure 1 Item 18, Col 4 Lines 51 – 58) coupled to the memory circuitry and operative to discard (Col 5 Lines 48 – 53) certain ones of the data blocks received at the input ports in an oversubscription condition (Col 6 Lines 37 – 44 "comparison done by the controller") in which the received data block exceed a designated capacity (Figure 3B Item 110, Col 6 Lines 37 – 44) of the processor; wherein a discarded data block indicator is generated (Figure 3B Item 111, Col 6 Lines 45 – 54) for a given one of the input ports if a data block received at the given input port for a particular protocol data unit is discarded (Col 6 Line 67 – Col 7 Line 8); wherein one or more additional data blocks received at the given input port for the particular protocol data unit are discarded (Col 6 Line 67 – Col 7 Line 8 "discard cell") based at least in part on the discarded data block indicator (Figures 3A – 3B Items 101 and 112, Col 6 Line 67 – Col 7 Line 8); and

wherein the controller circuitry is operative to maintain a separate discarded data block indicator for each of the plurality of input ports (Figure 38 Items 111 – 112, Col 6 Lines 55 – 61).

As per claim 2, Lin also teaches wherein the controller circuitry sets the discard data block indicator for the given input port to a first value when a first data block of the particular protocol data unit is discarded (Col 6 Lines 45 – 54 "EPD flag").

As per claim 3, Lin also teaches wherein the controller circuitry is configured to automatically discard any remaining data block if the particular protocol data unit that are received at the given input port while the discarded data block indicator is set to the first value (Col 6 Line 62 – Col 7 Line 8).

As per claim 4, Lin also teaches wherein the discarded data block indicator for the given input port comprises a single bit (Figure 2 Item 36, Col 6 Lines 3 – 18).

As per claim 5, Lin also teaches wherein the single bit being at a first logic level indicates that at least one data block received at the given input port has been discarded (Figures 3A – 3B Items 112 – 115) for a corresponding protocol data unit (Figure 3B Item 114, Col 6 Lines 3 – 18, Lines 45 – 54), and the single bit being at a second logic level indicates that no data block received at the given input port has yet been discarded for the corresponding protocol data unit (Col 6 Lines 3 – 18 "CLP bit").

As per claim 7, Lin also teaches wherein the a given one of the discarded data block indicators (Col 6 Lines 3 – 18 "CLP bit") indicates whether or not at least one data block received at the corresponding input port has been discarded (Figure 3B Items 111 – 112, Col 6 Lines 55 – 61).

As per claim 8 Lin also teaches wherein after a final data block of the particular protocol data unit is received (Figure 3A Item 101) at the given input port while the discarded data block indicator for the given input port is set to the first value (Figure 3A Item 101, Col 6 Line 62 – Col 7 Line 8), the controller circuitry is operative to enqueue the particular protocol data unit in a protocol data unit buffer of the memory circuitry (Figure 3A Items 101 – 106, Col 7 Lines 9 – 19).

As per claim 9 – 10, Lin also teaches wherein the particular protocol data unit is enqueued with an associated error flag set (Figure 3A Item 103 "CLP=0", Col 7 Lines 9 – 19).

As per claim 11, Lin also teaches wherein the oversubscription condition is overcome by discarding only data blocks received at the given input port (Col 6 Lines 37 – 54 "stored cells associated with the particular virtual connection"), and associated with the particular protocol data unit (Figures 3A – 3B Items 108 and 115, Col 6 Line 62 – Col 7 Line 8).

As per claim 12, Lin also teaches wherein the received protocol data units (Figure 2 Item 20, Col 5 Line 54 – Col 6 Line 2) are associated with frame based data (Figure 2 Item 22, Col 5 Line 54 – Col 6 Line 2).

As per claim 13 – 14, Lin also teaches wherein at least one of the input ports comprises a physical input port of the processor (Figure 1 Item 12, Col 4 Lines 51 – 58); a logical input port of the processor (Figure 1 Item 12, Col 3 Line 64 – Col 4 Line 8).

As per claim 15, Lin also teaches wherein the protocol data unit (Figure 2 Item 20) comprises a packet (Figure 2 Item 22, Col 5 Line 54 – Col 6 Line 2).

As per claim 16, Lin also teaches wherein the processor is configured to provide an interface for communication of the received protocol data units between a network and a switch fabric (Figure 1 Item 16; The Examiner construes the output ports as a switch fabric, because it performs the switching function of routing pockets).

As per claim 17, Lin also teaches wherein the processor comprises a network processor (Figure 1 Item 18, Col 4 Lines 50 – 58 " a network", Col 6 Lines 24 – 36).

As per claim 18, Lin also teaches wherein the processor is configured as an integrated circuit (Figure 1 Item 10).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Franklin
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Art Unit 2181

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8/7/2006